

INTEGRATED CIRCUIT STRUCTURES INCLUDING EPITAXIAL SILICON
LAYERS IN ACTIVE REGIONS AND METHODS OF FORMING SAME

CLAIM FOR PRIORITY

5 This application claims priority to Korean Application No. 10-2002-0073869
filed November 26, 2002, the entire content of which is incorporated herein by
reference.

FIELD OF THE INVENTION

10 The present invention relates to semiconductor structures and methods of
forming the same. More particularly, the present invention relates to semiconductor
structures having isolation structures and methods of forming the same.

BACKGROUND

15 As semiconductor devices become highly integrated, issues such as leakage
current and punch through may arise. One way of addressing these issues is to use
silicon on insulator (SOI) substrate according to conventional technology as
illustrated in Fig. 1.

Referring to Fig. 1, a conventional SOI substrate has a structure where an
20 insulation layer 3 and a silicon layer 5 are sequentially stacked on a semiconductor
substrate 1. The insulation layer 3 is formed of a thermal oxide and the
semiconductor substrate 1 and the silicon layer 5 are formed of a silicon single
crystalline. In order to fabricate the SOI substrate, a first silicon substrate 1 having a
thermal oxide layer 3 is attached to a second silicon substrate 5, and then a lower part
25 of the second silicon substrate is removed by a planarization process. In a subsequent
process, a field oxide layer is formed to contact with the insulation layer 3 in the
silicon layer 5 to address the problem of leakage current that may occur during an
operation of a transistor. However, the SOI may be expensive since two silicon
wafers are used. Additionally, since a transistor is isolated by the insulation layer 3
30 and a field oxide layer, heat or a hot carrier may not be removed. Furthermore, it may
be difficult to apply a back bias.

According to another conventional technology, a path can be formed to
provide for the emission of heat or a hot carrier (or for applying a back bias) as
illustrated in Fig. 2. Referring to Fig. 2, the silicon layer 5 and the insulation layer 3

in Fig. 1 are sequentially patterned to form an opening partially exposing the semiconductor substrate 1. An epitaxial layer 7 is grown from the exposed semiconductor substrate 1 in the opening to fill the opening. As illustrated in Fig. 2, while the epitaxial layer 7 is grown, a defect (D) may occur at the insulation layer 3, and a void (V) may be formed in the epitaxial layer 7. In the case that the void (V) is very large, the epitaxial layer 7 may not provide an adequate electrical path between the silicon layer 5 and the semiconductor substrate 1. This may result in a reduction in the reliability of the semiconductor substrate.

SUMMARY

Embodiments according to the invention can provide integrated circuit structures that can include an isolation structure that electrically isolates an active region of an integrated circuit substrate from adjacent active regions and an insulation layer that extends from the isolation structure to beneath the active region. An epitaxial silicon layer can extend from the active region through the insulation layer to a substrate beneath the insulation layer.

In some embodiments according to the invention, the insulation layer can include a trench thermal oxide layer on an inner wall of a trench in the substrate. The insulation layer can extend through the inner wall of the trench to beneath the active region.

In some embodiments according to the invention, a nitride liner can be on the trench thermal oxide layer and a field oxide layer in the trench can be on the nitride liner. In some embodiments according to the invention, the nitride liner can extend through the inner wall into the insulation layer beneath the active region.

In some embodiments according to the invention, an impurity-doped region can be at an interface of the substrate and the epitaxial silicon layer. In some embodiments according to the invention, the insulation layer can be a thermal oxide. In some embodiments according to the invention, the active region can be a strained silicon crystalline structure.

In some embodiments according to the invention, the epitaxial silicon layer can be a first epitaxial silicon layer in the active region adjacent to and in contact with the inner wall of the trench. A second epitaxial silicon layer can be in the active region spaced apart from the first epitaxial silicon layer.

In other embodiments according to the invention, an epitaxial silicon layer can

be formed from an active region through a silicon layer having a strained crystalline structure to a substrate beneath the silicon layer. Then the silicon layer can be replaced with an insulation layer.

5 In some embodiments according to the invention, the silicon layer can be a silicon germanium layer. In some embodiments according to the invention, the silicon layer having the strained crystalline structure can be removed from beneath the active region to form a gap between the active region and the substrate and the insulation layer can be formed in the gap.

10 In some embodiments according to the invention, the epitaxial silicon layer can be formed from the active region through the silicon layer and another spaced apart silicon layer beneath the silicon layer having a strained crystalline structure to the substrate beneath the second silicon layer. The first and second silicon layers can be replaced with the first insulation layer and a second insulation layer respectively.

15 BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 illustrates a cross-sectional view of a conventional SOI substrate.

Fig. 2 illustrates a cross-sectional view of an SOI substrate according to a conventional technology.

20 Fig. 3 is a layout view that illustrates embodiments of integrated circuit structures according to the invention.

Fig. 4 is a cross-sectional view taken along a I-I' in Fig. 3 that illustrates embodiments of integrated circuit structures according to the invention.

Figs. 5A through 5E are cross-sectional views that illustrate embodiments of methods of forming integrated circuit structures according to the invention.

25 Fig. 5F is a cross-sectional view that illustrates embodiments of integrated circuit structures according to the invention.

Fig. 6 is a cross-sectional view taken along a I-I' in Fig. 3 that illustrates embodiments of integrated circuit structures according to the invention.

30 Fig. 7 is a layout view that illustrates embodiments of integrated circuit structures according to the invention.

Fig. 8 is a cross-sectional view taken along a II-II' in Fig. 7 that illustrates embodiments of integrated circuit structures according to the invention.

Fig. 9 is a layout view that illustrates embodiments of integrated circuit structures according to the invention.

Fig. 10 is a cross-sectional view taken along a III-III' in Fig. 9 that illustrates embodiments of integrated circuit structures according to the invention.

DESCRIPTION OF EMBODIMENTS ACCORDING TO THE INVENTION

5 The present invention will now be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and
10 complete, and will fully convey the scope of the invention to those skilled in the art.

 In the drawings, the thickness of layers and regions are exaggerated for clarity. It will be understood that when an element such as a layer, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present.

15 Furthermore, relative terms, such as "beneath", are used herein to describe one element's relationship to another as illustrated in the Figures. It will be understood that relative terms are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures. For example, if the device in the Figures is turned over, elements described as "beneath" other elements would be
20 oriented "above" the other elements. The exemplary term "beneath", can therefore, encompass both an orientation of above and below.

 It will be understood that although the terms first and second are used herein to describe various regions, layers and/or sections, these regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish
25 one region, layer or section from another region, layer or section. Thus, a first region, layer or section discussed below could be termed a second region, layer or section, and similarly, a second without departing from the teachings of the present invention. Like numbers refer to like elements throughout.

 Fig. 3 is a layout view that illustrates embodiments of integrated circuit
30 structures according to the invention. Fig. 4 is a cross-sectional view taken along a I-I' in Fig.3 that illustrates embodiments of integrated circuit structures according to the invention. Referring to Figs. 3 and 4, a field oxide layer (F_{OX}) 28 is on an integrated circuit substrate (such as a semiconductor substrate) 10 to define an active region (AR). A silicon layer 14 is on the active region (AR). An insulation layer (O) 24b is

beneath the silicon layer 14 between the silicon layer 14 and the substrate 10. Word lines (W) 32 cross over the active region (AR). A gate oxide layer 30 is between the word line (W) 32 and the silicon layer 14. A capping layer pattern 34 covers the word line (W) 32. An epitaxial layer 20 is extends from the silicon layer 14 through the
5 insulation layer 24b to the substrate 10 between the world lines (W) 32. An impurity-doped region 18 is between the epitaxial layer 20 and the substrate 10. A trench thermal oxide layer 24a is in a trench (in the substrate 10) between the field oxide layer (F_{OX}) 28 and the substrate 10 and between the field oxide layer (F_{OX}) 28 and the silicon layer 14. A nitride liner 26 is between the trench thermal oxide layer 24a and
10 the field oxide layer 28. In some embodiments according to the invention, the nitride liner 26 can be extended into the insulation layer 24b to beneath the active layer 14 as shown in Fig. 4.

Figs. 5A through 5E are cross-sectional views that illustrate embodiments of methods of forming integrated circuit structures according to the invention. Fig. 5F is
15 a cross-sectional view that illustrates embodiments of integrated circuit structures according to the invention.

Referring to Fig. 5A, a sacrificial layer 12 and a silicon layer 14 are sequentially formed on a substrate 10. The sacrificial layer 12 may be formed of silicon germanium (SiGe). A silicon germanium layer may be deposited on the
20 substrate 10 (having a silicon single crystalline structure). Since germanium has a larger atom size than silicon, the size of the lattice of the silicon germanium layer may be made to be greater than a silicon single crystalline by increasing the germanium concentration in the SiGe. Accordingly, when the silicon layer 14 is grown on the silicon germanium layer, the lattice of the silicon layer 14 may be broader than a
25 lattice associated with a silicon single crystalline structure, thereby allowing a transistor formed in the active area to have increased speed due to the strained lattice structure.

Referring to Fig. 5B, a mask pattern 16 is formed on the silicon layer 14. The mask pattern 16 can be formed of silicon nitride. The silicon layer 14 and the
30 sacrificial layer 12 are sequentially patterned using the mask pattern 16, thereby forming an opening 17 that exposes the substrate 10. The opening 17 may have a width that is greater than a depth of the opening 17. An impurity-doped region 18 is formed in the substrate 10 that is exposed by the opening 17 using the mask pattern 16.

Referring to Fig. 5C, an epitaxial layer 20 is grown from the substrate 10 exposed by the opening 17, thereby filling the opening 17. A silicon nitride layer is formed on the mask pattern 16 to cover the epitaxial layer 20. The silicon nitride layer and the mask pattern 16 are patterned to form a new mask pattern 16' which can be used to form a field oxide layer. The silicon layer 14, the sacrificial layer 12 and a portion of the substrate 10 are etched using the new mask pattern 16', thereby forming a trench 22.

Referring to Fig. 5D, the sacrificial layer 10 exposed by the trench is removed, thereby forming a gap between the silicon layer 14 and the substrate 10. In particular, the gap exposes a bottom surface of the silicon layer 14, a side wall of the epitaxial layer 20 and a top surface of the substrate 10. The etching process used to remove the sacrificial layer 12 may use a dry etch by supplying plasma of one or more of the following gases: hydrogen (H_2), oxygen (O_2), nitrogen (N_2) and fluoric compounds such as NF_3 and CF_4 , without applying a bias in a dry etch chamber. The etch process used to remove the sacrificial layer 12 may employ a wet etch using one or more of the following solutions: ammonia water (NH_4OH), hydrogen peroxide (H_2O_2), deionized water (H_2O), nitric acid (HNO_3) and fluoric acid (HF).

Referring to Figs. 5E and 5F, the exposed substrate 10 (where the sacrificial layer 12 has been removed) is thermally oxidized, thereby forming a trench thermal oxide layer 24a on an inner wall of the trench 22 and on the bottom of the trench 22. An insulation layer 24b is also formed by the thermal oxidation in the gap formed by removing the sacrificial layer 12. In some embodiments according to the invention, the insulation layer 24b may fill the gap where the sacrificial layer is removed. A nitride liner 26 is conformally deposited on the surface of the substrate 10. In some embodiments according to the invention, if the insulation layer 24b does not completely fill the gap, the nitride liner 26 may be formed on the insulation layer 24b beneath the active region 14.

In a subsequent process, the mask pattern 16' is removed, and a gate pattern including a gate oxide layer 30 and a word line 32 is formed on the silicon layer 14 as described in reference to Fig. 4. A capping layer pattern 34 is formed to cover the gate pattern.

Although not illustrated in Figures, impurities are implanted into the silicon layer 14 and the epitaxial layer 20 using the capping layer pattern 34 as an ion-implantation mask, thereby forming source/drain regions.

According to embodiments of the invention, the source/drain regions are connected to the insulation layer 24b, thereby allowing a reduction in capacitance therebetween. Also, the transistor may operate faster due to the strained silicon single crystalline structure of the silicon layer 14. The insulation layer 24b and the field oxide layer 28 can promote the electrical isolation of the transistor, thereby reducing leakage current. The epitaxial layer 20 can provide a path for heat or application of a back bias. Additionally, forming the epitaxial layer 20 before the insulation layer 24b may reduce defects and help reduce voids.

Fig. 6 is a cross-sectional view taken along a I-I' in Fig. 3 that illustrates embodiments of integrated circuit structures according to the invention. Referring to Fig. 6, an integrated circuit device includes two pairs of a silicon layers 14 (one pair on each side of the epitaxial layer) and two pairs of insulation layers 24b (one pair on each side of the epitaxial layer). The sacrificial layer 12 and the silicon layer 14 may be alternatively stacked on the substrate 10. Other elements can be as described above in reference to Figs. 3-5. The two insulation layers 24b may reduce leakage current and increase the speed of the transistor. It will be understood that the nitride liner 26 can be included in the gap between the active region and the substrate as a part of the insulation layer 24b.

Fig. 7 is a layout view that illustrates embodiments of integrated circuit structures according to the invention. Fig. 8 is a cross-sectional view taken along a II-II' in Fig. 7 that illustrates embodiments of integrated circuit structures according to the invention.

Referring to Figs. 7 and 8, an epitaxial layer (E) 20 is between the field oxide layer (F_{ox}) 28 and the word line (W) 32. An insulation layer 24b is between the silicon layer 14 and a substrate 10 and connected to a trench thermal oxide layer 24a. In some embodiments according to the invention, integrated circuit devices can be formed using methods discussed above in reference to Figs. 1-5, however, a patterned region of the sacrificial layer 12 and the silicon layer 14 may be different than that shown in Fig. 5A. It will be understood that the nitride liner 26 can be included in the gap between the active region and the substrate as part of the insulation layer 24b.

Fig. 9 is a layout view that illustrates embodiments of integrated circuit structures according to the invention. Fig. 10 is a cross-sectional view taken along a III-III' in Fig. 9 that illustrates embodiments of integrated circuit structures according to the invention.

Referring to Figs. 9 and 10, an epitaxial layer (E) 20 is on both sides of the word line (W) 32. The insulation layer 24b is between the substrate 10 and the silicon layer 14, and connected to the trench thermal oxide 24a beneath and along the word line (W) 32. In some embodiments according to the invention, integrated circuit devices can be formed using methods discussed above in reference to Figs. 1-5, however, a patterned region of the sacrificial layer 12 and the silicon layer 14 is different than that shown in Fig. 5A. It will be understood that the nitride liner 26 can be included in the gap between the active region and the substrate as part of the insulation layer 24b.

According to embodiments of the invention, the source/drain regions are electrically connected to the insulation layer, thereby allowing a reduction in capacitance therebetween. Also, the transistor may operate faster due to the strained silicon single crystalline structure of the silicon layer. The insulation layer and the field oxide layer can promote the electrical isolation of the transistor, thereby reducing leakage current. The epitaxial layer can provide an path for heat or application of a back bias. Additionally, forming the epitaxial layer before the insulation layer may reduce defects and help reduce voids.

Many alterations and modifications may be made by those having ordinary skill in the art, given the benefit of present disclosure, without departing from the spirit and scope of the invention. Therefore, it will be understood that the illustrated embodiments have been set forth only for the purposes of example, and that it should not be taken as limiting the invention as defined by the following claims. The following claims are, therefore, to be read to include not only the combination of elements which are literally set forth but all equivalent elements for performing substantially the same function in substantially the same way to obtain substantially the same result. The claims are thus to be understood to include what is specifically illustrated and described above, what is conceptually equivalent, and also what incorporates the essential idea of the invention.